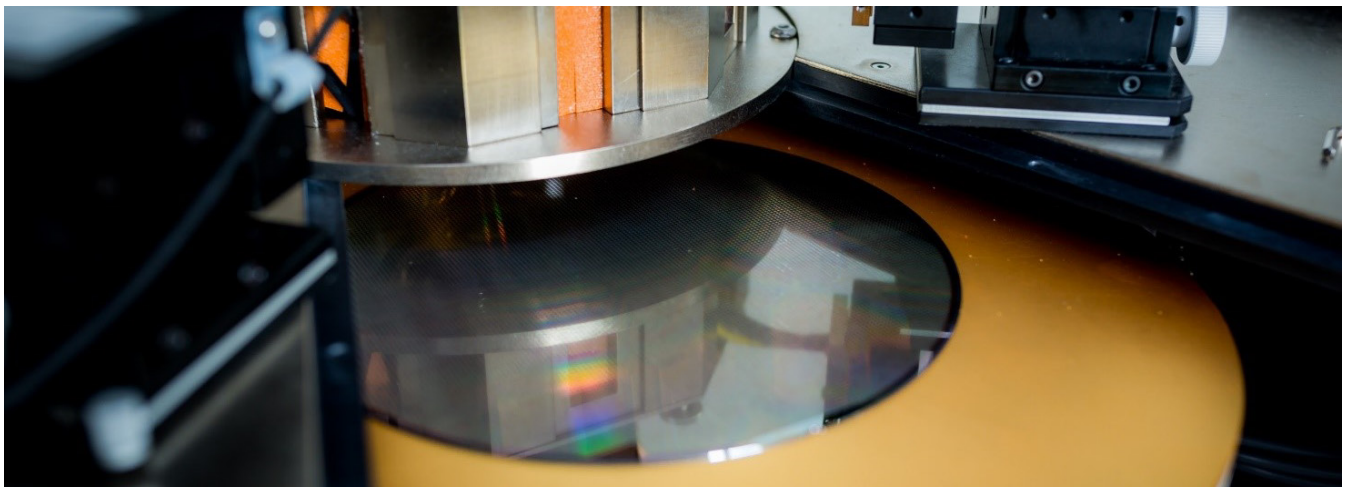
Fraunhofer
IIS

FRAUNHOFER INSTITUTE FOR INTEGRATED CIRCUITS IIS
DIVISION ENGINEERING OF ADAPTIVE SYSTEMS EAS

DEVICE CHARACTERIZATION ON WAFER LEVEL



© Fraunhofer IIS/EAS, Katharina Knaut

The reliability of integrated circuits and devices is a key criterion for safety-critical or long-lived applications, e.g. in automotive and industrial electronics. In order to investigate and minimize the impact of different wear-out mechanisms, electrical measurements on wafer level are required.

Fraunhofer IIS/EAS is offering characterization services with a particular focus on semiconductor reliability according to the common industry standards (AEC-Q, JEDEC) as well as to specific customer requirements. Moreover, we are offering additional measurements required for the calibration of degradation models.

Our Services:

- Preparation of test concepts and qualification plans
- Measurements on wafers (up to 12") and single dies (2x2 mm² to 10x10 mm², max. aspect ratio 3:1)
- Thermal qualification tests in a temperature range from -40°C until 300°C, temperature cycles possible
- Device testing up to a current of 120 mA at 1 kV / up to 1 A at 210 V
- Export and analysis of measurement data
- Risk analysis for new technologies
- Requalification of technologies

Selected Measurements

Gate Oxide Integrity (GOI)

Measurement according to JEDEC JESD35-A
- Voltage-ramp test incl. detection of voltage to breakdown
- Current-ramp or bounded J-ramp tests incl. detection of charge to breakdown and charge density to breakdown
- Weibull statistics and identification of extrinsic faults

Time-Dependent Dielectric Breakdown (TDDB)

Measurement according to JEDEC JESD92
- Constant voltage stress procedure at elevated temperature
- Observation of stress current and stress-induced leakage current
- Detection of hard and soft breakdowns
  - Time to breakdown
  - Charge to breakdown
  - Charge density to breakdown
- Weibull statistics including area and voltage scaling

Hot Carrier Injection (HCI)

Measurement according to JEDEC JP001, JESD28-A, JESD28-1 (NFET) and JESD60-A (PFET)
- Stress cycles with interim characterization
  - DC stress conditions
  - Monitoring of VTHI, VTHX, IDLIN, IDSAT and GMAX
- Evaluation of
  - Absolute or relative parameter shifts
  - Description by power law or logarithmic models
  - Lifetime prediction based on pre-defined degradation criteria and use conditions

Additional measurements for modeling support
- Impact of stress voltage
  - DC conditions with multiple combinations of Vds and Vgs
  - Custom AC (digital) and transient stress signals
- Impact of temperature
- Impact of device geometry
- Recording of complete I-V curves
- Application of further extrapolation models

Bias Temperature Instability (BTI)

Measurement according to JEDEC JP001, JESD90 (PFET NBTI) and JESD241 (fast BTI)
- Stress cycles with interim characterization
  - DC stress conditions at elevated temperature
  - Monitoring of VTHI, VTHX, IDLIN, IDSAT, GMAX in standard measurements or VTLIN/VTSAT in fast NBTI measurements
- Evaluation of
  - Absolute or relative parameter shifts
  - Description by power law models
  - Lifetime prediction based on pre-defined degradation criteria and use conditions

Additional measurements for modeling support
- Impact of stress voltage:
  Custom AC (digital) and transient stress signals
- Impact of temperature
- Impact of device geometry
- Recording of complete I-V curves and recovery traces
- Application of further extrapolation models

Fraunhofer Institute for Integrated Circuits IIS
Division Engineering of Adaptive Systems EAS
Zeunerstraße 38
01069 Dresden, Germany

Contact:
Dr. André Lange
+49 351 4640-764
andre.lange@eas.iis.fraunhofer.de

www.eas.iis.fraunhofer.de/en