

Joint interdisciplinary work to enable novel, industry-ready chiplet solutions

Chiplet Center of Excellence (CCoE)

Fraunhofer is going to establish the Chiplet Center of Excellence (CCoE), which is a unique research activity based on Fraunhofer's long experience and broad research portfolio in design, implementation and test of 2.5 and 3D integrated electronic systems. The Center aims at establishing a common understanding among the partners and at creating a suitable chiplet development methodology. This goal is supplemented by recommendations to shape a multi-vendor chiplet ecosystem. To support the success of this results in industrial practice, the methodological approaches are to be incorporated into standards.

The unique position of the CCoE results from the broad technological portfolio of Fraunhofer and the closely interlinked, interdisciplinary cooperation with industry. CCoE will be connected tightly to the European ECA pilot line "Advanced Heterogeneous System Integration" and it will be aligned with chiplet research activities in the pan-European alliance of research organizations.

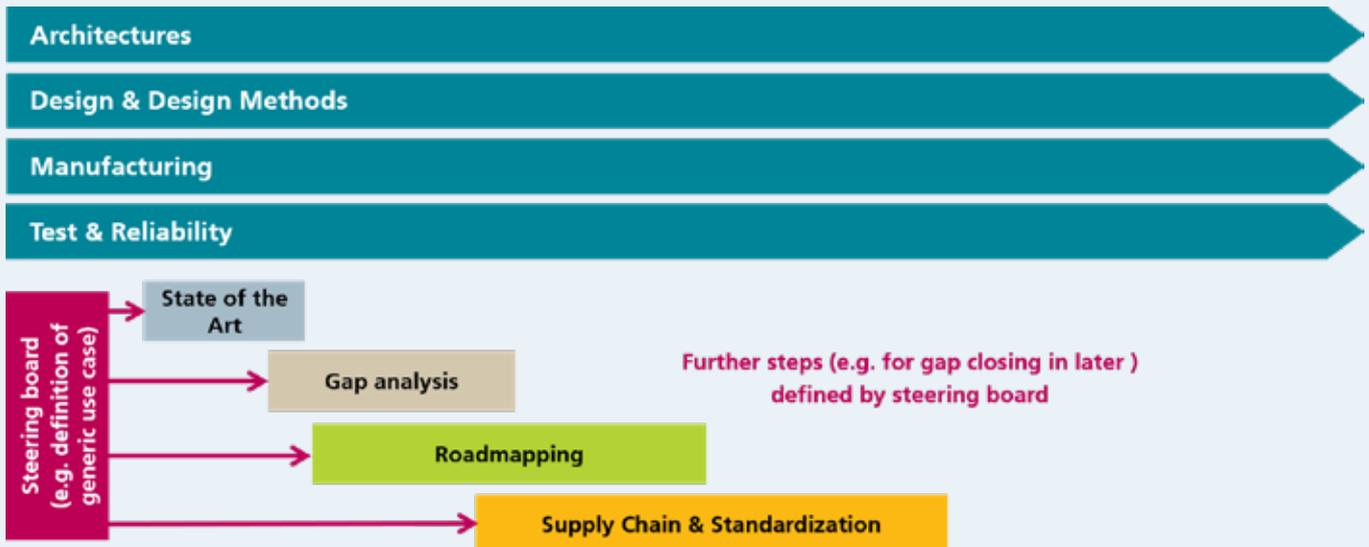
The joined work of Fraunhofer and its industrial partners focuses on strong European industrial sectors and will support competitiveness and technological sovereignty. For the first two years, starting 2024, the CCoE will focus on automotive applications and their specific requirements. All research activities in CCoE are defined, monitored and controlled by the participating industry. This will ensure the clear focus on industrial requirements. Based on these results, partners are able to derive differentiating projects for the development of their own products and technologies.

Strategic partnership benefits

- Greater **effectiveness and sharing of initial efforts** as part of a strong and focused network
- Access to **technology comparisons, variant analyses, application-specific roadmaps**, etc.
- Overview on **technological state-of-the-art** and research activities, w.r.t. use cases and application-specific requirements
- **Networking** with chiplet ecosystem (companies & research)
- Interdisciplinary approach of bringing together **experts** from design, tooling, technology and application **along the automotive value chain**
- Determination of **"Sweet Spots"** for use cases, based on application-centric requirements considering optimization criteria
- **Evaluation** of different **technology - architecture options** using fabricated test structures and sub-systems
- Interface to European **system integration pilot line**
- Joint work on **new technical standards** for chiplets and contribution to **relevant standardization committees**

Fast Facts

1. Long-term activity with initial 2-year phase focusing on automotive
2. Goal: Elaboration of guidelines and tool set for a development, manufacturing and test methodology for chiplets in automotive applications
3. Contribution of research results and elaborated methods into industry standards



CCoE agenda

The CCoE will **focus on** chiplets in **automotive** applications and their specific requirements. The research activities will start with a state-of-the-art review (commercial solutions as well as research) in order to identify which approaches and solutions are available today (and which are not) to realize advanced chiplet solutions. Therefore, the disciplines “architectures”, “design & design methods”, “manufacturing” and “test & reliability” are considered. Fraunhofer will capture the **state-of-the-art** in general and **specified for a generic use case** with basic functional structures, which are defined in the consortium. This is the basis for a gap analysis with regard to different optimization criteria (performance, cost, supply chain robustness, etc.).

For the use case, the industrial steering committee also defines sub-blocks for which most open questions arise in the interaction of various parameters such as substrate materials, package technologies and design implementation. Fraunhofer will carry out **variant analyses** based on the desired key target characteristics and will provide evaluations with the help of simulations and measured **hardware implementations**. The aim is to derive **proven recommendations** with regard to the critical parameters and design options. They are part of the elaboration of activities for gap closing, including the definition of roadmaps.

To establish a long-term chiplet platform, the hardware implementation of basic functions (die2die interface, memory integration, analog interfaces) and its evaluation concerning key characteristics will be essential to cover different complexities. These findings are incorporated into a **methodology for demonstrating the automotive suitability**. The goal is to elaborate a **guideline for the development, manufacturing and test** for chiplets in automotive applications as well as **building blocks and sub-architectures**. They can be widely **reused and adapted** to other applications. Proven building blocks and methods could also be contributed to international standardization activities.

Conditions for participation

- Participation is open for all companies along the automotive value chain (semiconductor suppliers, Tier 2, Tier 1, OEM).
- All research and development works in the consortium are pre-competitive.
- All results and findings obtained are available to all partners involved to the same extent.
- All partners obtain non-exclusive rights on all results created within the CCoE with the right to sublicense for industry partners (e.g. for the development/licensing of products).
- Industry partners may delegate employees as part of the joint research groups.
- The activities of CCoE are governed by a industry-centric steering committee (responsible for decisions about the research program, for the research focus and for the monitoring of the overall performance of CCoE).
- A technical board is composed of industry and Fraunhofer (responsible for the set up and run of technical working groups and for the preparation of decision templates).
- Access to the consortium and all results is possible with an annual access fee

Contact

Andy Heinig
 Fraunhofer Institute for Integrated Circuits IIS
 Division Engineering of Adaptive Systems EAS
 Tel. +49 351 45691-250
andy.heinig@eas.iis.fraunhofer.de
www.eas.iis.fraunhofer.de/en.html