THE DESIGN ENVIRONMENT FOR HETEROGENEOUS SYSTEMS

SystemC / SystemC AMS based Simulation and Modeling Technologies
Outline

- COSIDE® Today
- COSIDE® 2.0
- COSIDE® Future
Management Summary

- Combination of analog and mixed-signal hardware and software
- Integration of standard tools (Matlab, Cadence, Synopsys, etc.)
- HiL simulation, testing
- Large libraries
- Improved and extended analog solvers
- Generation of IP-protected customer models
- Formal verification
SystemC AMS
Language Principal and Base for COSIDE®

- **C++ based** Hardware description language for higher abstraction levels
- Hosted and **standardized** by the Accellera Systems Initiative (former OSCI)
- SystemC focuses on the description of digital hard- and software on higher abstraction levels
- SystemC AMS extends SystemC for abstract modeling of analog/mixed-signal
Modeling language comparison

- **Modelica** *(A)*
- **SystemC-AMS** *(A)*
- **SPICE** *(A)*

**SystemC/TLM** *(A/D)*

**SystemC-AMS** *(A)*

**Ptolemy**

* Std. Language
  (A) – mainly analog focused
  (D) – mainly digital focused
  (A/D) – mixed signal focus
The basic technology for the Accellera **SystemC AMS language standard** was developed by Fraunhofer IIS/EAS.

<table>
<thead>
<tr>
<th>Modeling method / language</th>
<th>Computing time for 1 sec real time</th>
</tr>
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<tbody>
<tr>
<td>Fast-Spice Simulator</td>
<td>1.000.000.000 sec → approx. 30 years</td>
</tr>
<tr>
<td>VHDL/VHDL-AMS</td>
<td>100.000 sec → approx. 1 day</td>
</tr>
<tr>
<td><strong>SystemC / SystemC AMS</strong></td>
<td>5 sec (Source: Dr. Georg Pelz – Infineon AG; Simulation of a window lifter)</td>
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**Advantage:** SystemC/SystemC AMS modeling technology enables the overall system simulation of application scenarios

**Downside:** Technology is complex and modeling effort is high
Design Environment based on SystemC / SystemC AMS

- Powerful Modeling Capabilities
- Schematic Design Entry
- Accellera System Initiative Compliant
- Full TLM 2.0 Support
- SystemC / VHDL Mixed Language Modeling
- Basic Model Libraries
- Profiling Performance and Memory Leakages, Model & TB Generation
- Designed by the Developers of the SystemC AMS Proof-of-Concept Library
Customer Advantages

- Improved modelling efficiency
- Higher model quality
- Low entry level
- Improved maintainability
- Enabling model reuse
- Extended model (re)use cases
- License-free simulation
Schematic Editor

- Eclipse integrated (GMF/GEF based)
- Double click to source file, hierarchy browsing
- Autorouting – also if modules moved
- Improved parameter handling
- Advanced editing features
- Advanced Copy&Paste
- Printing and svg, png, … export
TLM Modeling Support

- Full TLM 2.0 Support
- Additional TLM generic library (full TLM 2.0 compliant)
XML-Editor Frontend / Code completion

- Easy model definition via XML editor frontend
- SC/SCA Syntax highlighting
- Code completion with suggestions
Simulation Control, Debugging

- **SCSimCtrl**: Advanced Drag’n’Drop Trace Selection, Hierarchy Browsing and Simulation Control
- Debugging Facilities in Stand-alone as well as in Coupled Simulation Scenarios
COSIDE® Easy Tool Coupling

Tool Couplings for model exchange and implementation level verification

- **Customer Model Generation** with ensured IP-Protection
- **Model Exchange** with reproducible analogue simulation behavior
- **Hardware in the Loop Simulation** with dSPACE, ZedBoard (ARM®)

Co-Simulation Framework

- COSIDE® @Lab Hardware
- Vector Informatik CANoe
- dSPACE HiL/RCP Hardware
- MathWorks MatLab/ Simulink
- Synopsys Saber
- Cadence NCSim
- Mentor ModelSim/ Questa
Direct SystemC AMS HiL-Simulation

Test of Component Specification (e.g. for IC’s)

Test of Hardware Components in a not yet existing environment

SystemC AMS Model

ds1006.x86

dSPACE

Source: dSPACE

Test of Component Specification (e.g. for IC’s)

Test of Hardware Components in a not yet existing environment

Source: dSPACE
SystemC HiL-Testing with COSIDE® @Lab

- Setup SystemC UVM high level Regression Tests
- COSIDE® @Lab: reuse Testbench for Prototype Validation in the Laboratory
- Integrate Lab. Equipment via RS232, GPIB etc.
State Chart Editor

- UML based State Chart design entry
- Code generation backend
State Chart Code generation

Code Generator

Statechart

XML

Java/XSLT

SystemC behavioral

Controller C-code

NuSMV

Back annotation

target specific backend:

complex operations: design rule checks, automated verification, model transformations, e.g. remove complex structures, hierarchy flatten, preprocessing, ...

simplified statechart

counter examples

Hierarchic statechart
Formal Verification of State Charts

Formal Checker

Back Annotation
SystemC AMS Libraries

- Library with approx. 130 basic elements
- Optimized Line models
- Failure Injection
- Statistical Simulation
- Regression Test Concept
- Architecture Select
- Signal bundles / Abstract signals / Reconnect signals from test bench
- Tracing and Object access via pattern matching
- Easily usable TLM Library with debug feature
COSIDE 2.0

The Design Environment for Heterogeneous Systems

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Institut Integrierte Schaltungen - EAS Dresden
COSIDE 2.0 - Highlights

- Eclipse 4 based
- New Model libraries
- Completely SystemC AMS 2.0 compliant
- Model templates
- Documentation
- Example Projects
- Improved usability
- Screen casts for typical use cases
Piece Wise Linear (PWL) SystemC AMS Extension

- Fast and robust modelling of diodes
- Modelling of switched networks, pwm stages, ...
- Modelling of slew rates
SystemC / SystemC AMS Spice Integration

- Mixing Spice and SystemC-AMS ELN modules
- Spice linked to SystemC-AMS kernel
- SystemC-AMS Spice modules or embedded
  Spice description (subcircuits) and modelcards
RF – SystemC / SystemC AMS Libraries

- RF modelling at system level
- Library of basic elements
Mechanical SystemC AMS Library

- Fast and robust models
- Basics for modelling mechanical environments
Library Licensing

- Pre-compiled inside larger models, distribution always allowed
- Apache – source code available
- COSIDE Open License – Source code available – distribution is allowed pre-compiled only
- COSIDE License – no source code available
Library Model Import

- Green and yellow signed models can be imported into the current project
- They can be renamed and adopted
- They can be used as templates for own primitive models
Library Documentation

- Short description preview
- Direct access via menu
- Completely re-worked and improved
Example Projects

- Examples with typical use cases and modelling techniques

- Import into current workspace

- Models or libraries can be used as templates via copy model / library function
PDF based documentation

Completely re-worked and re-structured
Screen Casts

start the simulation
System level tool-suite for modelling, design, verification and integration of HW/SW mixed signal systems
COSIDE - Future

- Verification
- UVM-SystemC (AMS) integration
- Model Libraries
- Documentation / Usability

- Cooperation with partners

- Your requests
THANK YOU FOR YOUR ATTENTION
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