THE DESIGN ENVIRONMENT FOR HETEROGENEOUS SYSTEMS

COSIDE® Use Cases & Applications
Verification

Collaboration

Mixed Signal
Architecture and System Level Design

Model Exchange

Co-Simulation

Regression Testing
COSIDE® Creates
COSIDE® – Creates Virtual prototype

- Easy model definition via XML editor frontend
- SC/SCA Syntax highlighting
- Code completion with suggestions
Create model database

- Easy model definition via XML editor frontend
- SC/SCA Syntax highlighting
- Code completion with suggestions
- Creates

Model database – SystemC code generation

DB → SC/SCA → Primitive
DB → TB → Test bench
DB → Doc → Documentation
Plain SystemC AMS – Simple DC/DC buck converter
COSIDE® – Creates
Plain SystemC AMS – Simple DC/DC buck converter (top-level)
COSIDE® Verifies
Verifies

Test bench infrastructure

DB

Simple

Generic

UVM

COSIDE® Regression test framework

Interactive workbench
- Apply simple stimulus to a design under test (e.g. sub-system)
- Apply multiple test cases to a design under test (e.g. top-level)
- Add measurement, connection, injection utilities for each TC
Verifies UVM test bench

- Apply UVM structure to a design under test (e.g. top-level)
- Using Scoreboard, Virtual Sequencer, Driver, Monitor, Agents etc.
Interactive workbench

- Compile & select Traces
- Design/Adapt
- Run & Trace
- Control
- Visualize
Plain SystemC AMS – Simulation results

- Verifies
COSIDE® – Verifies
Regression test framework

Flexible and user adaptable regression infrastructure.
COSIDE® Connects
Model database – Co-Simulation interface gen.

- **SC/SCA** (Primitive)
- **TB** (Test bench*)
- **IF** (Coupling)
- **Doc** (Documentation)
- **Schematic**
- Customer Model Generation with ensured IP-Protection

- Model Exchange with reproducible analogue simulation behavior

- Hardware in the Loop (HiL) Simulation with dSPACE, ZedBoard (ARM®)

Tool Couplings for model exchange and implementation level verification
Tool Couplings for implementation level verification **Mentor Questa**

Easy to achieve by RMB to entity xml and let COSIDE® do the work

**Coupling menu**
- Questa coupling
- Create co-simulation interface
- Create VHDL test bench
Connects
Co-Simulation framework – Refinement and implementation (2)
Tool Couplings for implementation level verification with **Cadence AMS Designer**

Easy to achieve by RMB to entity xml and let COSIDE® do the work

**Coupling menu**

- AMS Designer (NCSim) coupling
- Create co-simulation interface
- Create VHDL/Verilog test bench
Co-Simulation framework – Refinement and implementation (4)
**Concept phase** – SystemC virtual prototype (plain SystemC)

**Implementation phase** – Reuse of SystemC tests for RTL model regression testing (Co-Simulation)

**Hardware validation** phase – Reuse of SystemC tests for FPGA/ASIC regression testing (COSIDE® @ Lab. – dSPACE, ZedBoard)
– **Connects**

Co-Simulation framework – Bridge the missing link

Implementation designer provide module entity

Generate initial schematic – contains specified entity
Adding predefined interface modules to match the entity and establish the link between system-level and implementation.
Tool Couplings for model exchange with **Matlab Simulink**

Easy to achieve by RMB to entity xml and let COSIDE® do the work

Coupling menu

- Simulink coupling
- Create co-simulation interface and a Simulink symbol
Co-Simulation framework – Customer model (2)
COSIDE® Collaborates
- **Collaborates**

IP protected model exchange

- TIER-2
- TIER-2
- TIER-2

**tight cooperation**

- TIER-1
- TIER-1

**tight cooperation**

- IP protected
- source code

**e.g. automotive value chain**

- OEM
Mercurial

Subversion

CVS

Clear Case

Git

Design Sync

Integrated version management support
COSIDE® thanks for your attention!

Questions

Discussions

Suggestions

Feature requests
THANK YOU FOR YOUR ATTENTION
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