Fraunhofer IIS/EAS supports its customers in various challenges of advanced packaging technologies from system-in-package (SIP) to 3D-integration. We offer a wide range of design services and accompany your 3D projects from concept to the first prototype. More than ten years of our experience and successful projects are the basis to use the new technological opportunities.

We develop design tools, models, simulation and optimization methods for innovative system and packaging solutions. Accelerate the introduction of advanced packaging and solve the challenges in cooperation with us.

**Our Services**

- Identification of application-optimized integration technology (from SIP and embedded wafer level packaging to die stacking with through-silicon vias (TSV))
- Design support from system planning to implementation
- Case studies for cost and performance estimation
- Interposer design
- 3D floorplanning
- Modeling of multi-physical effects (e.g., heat transfer)
- Planning and management of prototype manufacturing at our partners

**Your Benefits**

- Higher system performance and lower power consumption
- Miniaturization of complex systems
- Reduced design costs compared to ASIC development
- Reduced risk for the introduction of 3D integration technologies in your products because of our longtime experience
- One contact from system concept and design to the development of prototypes
References and Partners

In cooperation with reputable companies, such as Infineon, Sintef or Seleon, we already applied advanced packaging technologies to first prototypes:

- Integration of image sensors and processors
- Automotive tire pressure sensor
- Wireless ECG sensor in SIP technology

Our customers emphasize reliability and robustness. Most of them are related to the following application domains:

- Wireless communications
- Automotive industry
- Medical technology

New Opportunities and Challenges

Traditional integration of complex system-on-chip reaches its technological and commercial limits with increasing system functionality and the growing demand of miniaturization. The partitioning of a system into a stack of dies allows higher data rates and lower power consumption by shortening the length of signal lines. Furthermore it enables the tight integration of different modules, such as processors, sensors and wireless interfaces into a device.

Special challenges of the design of 3D systems are the handling of system complexity, the optimal implementation in a wide design space with various technological options as well as the consideration of thermal, mechanical and electrical effects in the tightly integrated stack.

About Us

The Fraunhofer Institute for Integrated Circuits IIS performs contract research and development in the fields of microelectronic systems and software. The researchers of its Design Automation Division EAS in Dresden develop methods and tools for the reliable computer-aided design of complex electronic and mechatronic systems. A faster implementation and optimization of integrated circuits, electronic devices and complex sensor systems is the aim of all research activities in order to reduce a product’s time-to-market.

Furthermore, the scientists work on own innovative technologies and systems. An important task of all activities is to bridge the gap between novel manufacturing technologies and system level design.

Variety of Technologies for Integration of Multiple Dies Within a Package

**system-in-package**
- Placement of different IC at package substrate
- Wire bond or flip-chip connection
- Integration of passive devices

**interposer-based integration**
- Higher integration level using thinned silicon interposers
- Signal routing between dies within the metal layers of interposers and its TSV

**direct stacking**
- Highest integration density
- Extremely short interconnects
- Requires die and stack co-design

1 Wireless ECG sensor with SIP technology